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1 Task scheduling and real-time: Task-level timing models for guaranteed performance in multiprocessor networks-on-chip

P. Poplavko, T. Basten, M. Bekooij, J. van Meerbergen, B. Mesman

October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**

Full text available: pdf(299.73 KB) Additional Information: full citation, abstract, references, index terms

We consider a dynamic application running on a multiprocessor network-on-chip as a set of independent jobs, each job possibly running on multiple processors. To provide guaranteed quality and performance, the scheduling of jobs, jobs themselves and the hardware must be amenable to *timing analysis*. For a certain class of applications and multiprocessor architectures, we propose *exact timing models* that effectively co-model both the computation and communication of a job. The models ...

Keywords: buffer minimization, data flow graph, network-on-chip, performance evaluation, real-time, system-on-chip

2 Data and memory optimization techniques for embedded systems

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg

April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2

Full text available: pdf(339.91 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of optimizati ...

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

3 Execution-driven simulation of multiprocessors: address and timing analysis

S. Dwarkadas, J. R. Jump, J. B. Sinclair
October 1994 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 4 Issue 4

Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, citings, index terms

This article describes and evaluates an efficient execution-driven technique for the simulation of multiprocessors that includes the simulation of system memory and that is driven by real program work loads. The technique produces correctly interleaved address traces at run-time without disk access overhead or hardware support, allowing accurate simulation of the effects of a variety of architectural alternatives on programs. We have implemented a simulator based on this technique that offe ...

Keywords: distributed systems, execution-driven simulation, parallel tracing, shared-memory multiprocessors

4 Multiprocessor experiments for high-speed ray tracing
Severin Gaudet, Richard Hobson, Pradeep Chilka, Thomas Calvert
July 1988 **ACM Transactions on Graphics (TOG)**, Volume 7 Issue 3

Full text available: pdf(2.82 MB) Additional Information: full citation, abstract, references, citings, index terms

New single- and multiprocessor models for ray tracing are presented. Important features are (1) the use of custom VLSI building blocks, (2) the use of a modified hierarchical data-structure-based ray tracing algorithm with three disjoint data sets, and (3) scene access through adaptive information broadcasting. A modular design is presented that permits incremental performance enhancement up to two orders of magnitude over conventional minicomputers or workstations. Ray tracing is a surpris ...

5 A data acquisition methodology for on-chip repair of embedded memories
Dirk Niggemeyer, Elizabeth M. Rudnick
October 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 4

Full text available: pdf(258.34 KB) Additional Information: full citation, abstract, references, index terms

Systems-on-Chips often contain a large amount of embedded memory. In order to obtain sufficiently high yield, efficient diagnosis and repair facilities are needed for the memories. A novel and efficient approach for collecting complete failure data during on-chip memory testing is proposed that can be combined with a row/column reconfiguration algorithm for complete on-chip memory repair. A sequence of diagnostic tests of linear order is utilized that detects and localizes all cells involved in ...

Keywords: Diagnosis, built-in self-test, column failures, coupling faults, embedded memory, march tests, memory test, on-chip repair

6 A Network Traffic Generator Model for Fast Network-on-Chip Simulation
Shankar Mahadevan, Federico Angiolini, Michael Storgaard, Rasmus Grondahl Olsen, Jens Sparso, Jan Madsen
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 2**

Full text available: pdf(151.06 KB) Additional Information: full citation, abstract

For Systems-on-Chip (SoCs) development, a predominant part of the design time is the simulation time. Performance evaluation and design space exploration of such systems in bit- and cycle-true fashion is becoming prohibitive. We propose a traffic generation (TG) model that provides a fast and effective Network-on-Chip (NoC) development and

debugging environment. By capturing the type and the timestamp of communication events at the boundary of an IP core in a reference environment, the TG can su ...

7 Improving cache performance with balanced tag and data paths

Jih-Kwon Peir, Windsor W. Hsu, Honesty Young, Shauchi Ong

September 1996 **Proceedings of the seventh international conference on Architectural support for programming languages and operating systems**, Volume 31 , 30 Issue 9 , 5

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms

There are two concurrent paths in a typical cache access --- one through the data array and the other through the tag array. The path through the data array drives the selected set out of the array. The path through the tag array determines cache hit/miss and, for set-associative caches, selects the appropriate line from within the selected set. In both direct-mapped and set-associative caches, the path through the tag array is significantly longer than that through the data array. In this paper ...

8 Thermal Modeling, Characterization and Management of On-Chip Networks

Li Shang, Li-Shiuan Peh, Amit Kumar, Niraj K. Jha

December 2004 **Proceedings of the 37th annual International Symposium on Microarchitecture**

Full text available: pdf(551.38 KB) Additional Information: full citation, abstract

Due to the wire delay constraints in deep submicron technology and increasing demand for on-chip bandwidth, networks are becoming the pervasive interconnect fabric to connect processing elements on chip. With ever-increasing power density and cooling costs, the thermal impact of on-chip networks needs to be urgently addressed. In this work, we first characterize the thermal profile of the MIT Raw chip. Our study shows networks having comparable thermal impact as the processing elements and contr ...

9 Low-power: Latency and energy aware value prediction for high-frequency processors

Ravi Bhargava, Lizy K. John

June 2002 **Proceedings of the 16th international conference on Supercomputing**

Full text available: pdf(256.94 KB) Additional Information: full citation, abstract, references, citings, index terms

This work addresses the issues of access latency and energy consumption in value predictor design for high-frequency, wide-issue microprocessors. Previous value prediction research allows for generous assumptions regarding table configurations and access conditions, while ignoring prediction latencies and energy issues. However, the latency of a high-performance value predictor cannot always be completely hidden by the early stages of the instruction pipeline as previously assumed, and it causes ...

Keywords: complexity-effective design, data speculation, low power, trace cache processors

10 Parallel logic simulation of VLSI systems

Mary L. Bailey, Jack V. Briner, Roger D. Chamberlain

September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3

Full text available: pdf(3.74 MB) Additional Information: full citation, abstract, references, citings, index terms

Fast, efficient logic simulators are an essential tool in modern VLSI system design. Logic simulation is used extensively for design verification prior to fabrication, and as VLSI systems grow in size, the execution time required by simulation is becoming more and

more significant. Faster logic simulators will have an appreciable economic impact, speeding time to market while ensuring more thorough system design testing. One approach to this problem is to utilize parallel processing, taking ...

Keywords: circuit structure, parallel architecture, parallelism, partitioning, synchronization algorithm, timing granularity

11 Reliability and security: Hardware assisted control flow obfuscation for embedded processors

Xiaotong Zhuang, Tao Zhang, Hsien-Hsin S. Lee, Santosh Pande

September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: pdf(275.14 KB) Additional Information: full citation, abstract, references, citings, index terms

With more applications being deployed on embedded platforms, software protection becomes increasingly important. This problem is crucial on embedded systems like financial transaction terminals, pay-TV access-control decoders, where adversaries may easily gain full physical accesses to the systems and critical algorithms must be protected from being cracked. However, as this paper points out that protecting software with either encryption or obfuscation cannot completely preclude the control flo ...

Keywords: control flow graph, obfuscation

12 The Clipper processor: instruction set architecture and implementation

W. Hollingsworth, H. Sachs, A. J. Smith

February 1989 **Communications of the ACM**, Volume 32 Issue 2

Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

13 Efficient power co-estimation techniques for system-on-chip design

Marcello Lajolo, Anand Raghunathan, Sujit Dey

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(124.92 KB) Publisher Site Additional Information: full citation, references, citings, index terms

14 Challenges in the Design of a Scalable Data-Acquisition and Processing System-on-Silicon

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(155.29 KB) Publisher Site Additional Information: full citation, abstract

Increasing complexity of the functionalities and the resultant growth in number of gates integrated in a chip coupled with shrinking geometries and short cycle time requirements bring in several challenges into the design of present day VLSI chips. In this paper we present the challenges faced and the approaches successfully adopted in the design of a complex 2.5 million gate high bandwidth data acquisition and processing VLSI chip (a trace-

receiver chip, code-named Drishti) in a deep sub-micron ...

15 Special session on reconfigurable computing: Reconfigurable platforms for ubiquitous computing

Manfred Glesner, Thomas Hollstein, Leandro Soares Indrusiak, Peter Zipf, Thilo Pionteck, Mihail Petrov, Heiko Zimmer, Tudor Murgan

April 2004 **Proceedings of the 1st conference on Computing frontiers**

Full text available: pdf(479.97 KB) Additional Information: full citation, abstract, references, index terms

Ubiquitous computing requires flexibilty. Melting distributed electronic devices into everyday's life implies the need to adapt to evolving standards and dynamic environments. Furthermore, to gain user acceptance, such devices should be able to adapt to different usage patterns and user profiles. Scalability is also an important issue, allowing functional enhancements to already deployed systems. In this work we address these issues applying the concept of reconfigurability on different abstract ...

Keywords: communication, dynamic power management, networks-on-chip, reconfigurable hardware, reconfigurable processors, reconfiguration, ubiquitous computing

16 Optimal allocation of on-chip memory for multiple-API operating systems

D. Nagle, R. Uhlig, T. Mudge, S. Sechrest

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture**, Volume 22 Issue 2

Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references, citings, index terms

The allocation of die area to different processor components is a central issue in the design of single-chip microprocessors. Chip area is occupied by both core execution logic, such as ALU and FPU datapaths, and memory structures, such as caches, TLBs, and write buffers. This work focuses on the allocation of die area to memory structures through a cost/benefit analysis. The cost of memory structures with different sizes and associativities is estimated by using an established area model for on ...

17 An effective on-chip preloading scheme to reduce data access penalty

Jean-Loup Baer, Tien-Fu Chen

August 1991 **Proceedings of the 1991 ACM/IEEE conference on Supercomputing**

Full text available: pdf(1.18 MB) Additional Information: full citation, references, citings, index terms

18 Cache Memories

Alan Jay Smith

September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings, index terms

19 System synthesis of synchronous multimedia applications

Gang Qu, Miodrag Potkonjak

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: pdf(286.29 KB) Additional Information: full citation, abstract, references, index terms

Modern system design is being increasingly driven by applications such as multimedia and wireless sensing and communications, which have intrinsic quality of service (QoS)

requirements, such as throughput, error-rate, and resolution. One of the most crucial QoS guarantees that the system has to provide is the timing constraint among the interacting media (synchronization) and within each media (latency). We have developed the first framework for system design with timing QoS guarantees. In parti ...

Keywords: high-level embedded systems synthesis, on-chip memory minimization, synchronization

20 Modeling issues in the design of embedded systems: An IDF-based trace transformation method for communication refinement

Andy D. Pimentel, Cagkan Erbas

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(186.11 KB) Additional Information: full citation, abstract, references, citings, index terms

In the Artemis project, design space exploration of embedded systems is provided by modeling application behavior and architectural performance constraints separately. Mapping an application model onto an architecture model is performed using trace-driven co-simulation, where event traces generated by an application model drive the underlying architecture model. The abstract communication events from the application model may, however, not match the architecture-level communication primitives. T ...

Keywords: communication refinement, design space exploration

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